**Preliminary DATA SHEET**

**CFORTH-X2-10GB-ER**

***10GBASE-ER X2 Transceiver***

## CFORTH-X2-10GB-ER Overview

CFORTH-X2-10GB-ER 10GBd X2 optical transceivers are designed for Storage, IP network and LAN, it is a hot pluggable module in the Z-direction that is mainly usable in typical router/switches line card applications. The CFORTH-X2-10GB-ER is a fully integrated 10.3 Gb/s optical transceiver module that consists of a 1550nm wavelength optical transmitter and receiver, XAUI interface, Mux and Demux with clock and data recovery (CDR). In addition, they comply with the X2 Multi Sourcing Agreement (MSA).

## Product Features

- Up to 10 GBd bi-directional data links.
- Compliant with IEEE 802.3ae, 10GBASE-ER application.
- Compliant with X2 MSA.
- Temperature stabilized EML transmitter.
- PIN Photo-detector.
- XAUI electrical interface: 4 lanes @ 3.125 GBd.
- MDIO, DOM (Digital Optics Monitoring) support.
- Hot Z-Pluggable.
- SC Connectors
- Up to 40km on SMF
- Power Supply: 5V/3.3V/Adaptable Power Supply (APS: 1.2V)
- RoHS Compliance
- Operating temperature range: 0℃ to 70℃.

## Applications

- 10 GBd Ethernet

## Ordering Information

| *Part Number* | *Description* |
|---|---|
| CFORTH-X2-10GB-ER | 10GBASE-ER X2 Transceiver, SC Connectors, 1550nm, SingleMode Fiber 40km |

**Absolute Maximum Ratings**

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| Storage Ambient Temperature | $T_S$ | – 40 | | 85 | ℃ | |
| Supply Voltage (5V) | $V_5$ | 0 | | 6 | V | |
| Supply Voltage (3.3V) | $V_3$ | 0 | | 4 | V | |
| Supply Voltage (APS) | $V_{APS}$ | 0 | | 1.5 | V | |
| Optical Receiver Input | $P_{IMAX}$ | | | 1.5 | dBm | Average |

**General Specifications**

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| Data Rate | *DR* | | 10.3125 | | GBd | |
| Bit Error Rate | *BER* | | | $10^{-12}$ | | |
| Total Power Consumption | *P* | | | 4 | W | |
| Supply Voltage (5V) | $V_{CC5}$ | 4.75 | 5 | 5.25 | V | Operating Environment |
| Supply Voltage (+3.3V) | $V_{CC3}$ | 3.14 | 3.3 | 3.47 | V | Operating Environment |
| Supply Voltage (APS) | $V_{CCAPS}$ | 1.152 | 1.2 | 1.248 | V | Operating Environment |
| Supply Current (5V) | $I_{CC5}$ | | | 350 | mA | |
| Supply Current (+3.3V) | $I_{CC3}$ | | | 300 | mA | |
| Supply Current (APS) | $I_{CCAPS}$ | | | 1000 | mA | |
| Case Operating Temperature | $T_C$ | 0 | | 70 | ℃ | |

**Link Distances**

| *Parameter* | *Fiber Type* | *Distance Range (Km)* |
|---|---|---|
| 9.95 – 10.5 GBd | 9/125um SMF | 40 |

**Optical Characteristics - Transmitter**

***$V_{CC5}$=4.75V to 5.25V, $V_{CC3}$=3.14V to 3.47V, $V_{CCAPS}$=1.152V to 1.248V, $T_C$=0℃ to 70℃***

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| Optical Wavelength | $\lambda$ | 1530 | | 1570 | nm | |
| Launch Power | $P_{OUT}$ | – 4.7 | | 4.0 | dBm | Average |
| Launch Power of OFF Transmitter | $P_{OUT_OFF}$ | | | – 30 | dBm | Average |
| Side Mode Suppression Ratio | *SMSR* | 30 | | | dB | |
| Spectral Width (– 20 dB) | $\Delta\lambda$ | | | 0.6 | nm | |
| Optical Extinction Ratio | *ER* | 8.2 | | | dB | |
| Optical Return Loss Tolerance | $ORL_T$ | | | 12 | dB | |
| Relative Intensity Noise | *RIN* | | | – 128 | dB/Hz | |
| Transmitter Dispersion Penalty | *TDP* | | | 2 | dB | |
| Transmitter Reflectance | $TR_{TX}$ | | | – 12 | dB | |
| Eye Mask Definition | According to IEEE 802.3ae | | | | | |

**Optical Characteristics - Receiver**

***$V_{CC5}$=4.75V to 5.25V, $V_{CC3}$=3.14V to 3.47V, $V_{CCAPS}$=1.152V to 1.248V, $T_C$=0℃ to 70℃***

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| Center Wavelength Range | $\lambda_C$ | 1260 | | 1600 | nm | |
| Optical Input Power | $P_{IN}$ | – 15.8 | | –1.0 | dBm | Average, Informative |
| Receiver Sensitivity in OMA | $P_{IN_OMA}$ | | | – 14.1 | dBm | Informative |
| Stressed Receiver Sensitivity | $P_{IN_S}$ | | | – 11.3 | dBm | |
| Receive Reflectance | $TR_{RX}$ | | | – 12 | dB | |
| Loss of Signal Assert Level | $P_{LOS_A}$ | – 25 | | | dBm | |
| Loss of Signal DeAssert Level | $P_{LOS_D}$ | | | – 17 | dBm | |
| Loss of Signal Hysteresis | $P_{LOS_H}$ | 1 | | | dBm | |
| Receiver electrical 3dB upper cutoff frequency | *FR* | | | 12.3 | GHz | |

**Optical Characteristics – Stressed Signal Calibration**

***$V_{CC5}$=4.75V to 5.25V, $V_{CC3}$=3.14V to 3.47V, $V_{CCAPS}$=1.152V to 1.248V, $T_C$=0℃ to 70℃***

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| Vertical Eye Closure Penalty | | 2.2 | | | dB | |
| Stressed Eye Jitter | | 0.3 | | | $UI_{PP}$ | |

**Electrical Characteristics - DC**

***$V_{CC5}$=4.75V to 5.25V, $V_{CC3}$=3.14V to 3.47V, $V_{CCAPS}$=1.152V to 1.248V, $T_C$=0℃ to 70℃***

| *Parameter* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Remarks* |
|---|---|---|---|---|---|---|
| **A.** | | | | | | |
| **1.2V COMS I/O DC Characteristics (PRTAD; LASI; RESET; TX_ON/OFF)** | | | | | | |
| External Pull-Up Resistor For Open Drain | $R_{PU}$ | 10 | | 22 | kΩ | |
| Output High Voltage | $V_{OH}$ | 1 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.15 | V | |
| Input High Voltage | $V_{IH}$ | 0.84 | | 1.2 | V | |
| Input Low Voltage | $V_{IL}$ | | | 0.36 | V | |
| Input Pull-Down Current | $I_{PD}$ | 20 | | 120 | uA | $V_{IN}$=1.2V |
| **B.** | | | | | | |
| **XAUI I/O DC Charateristics (TXLANE[0..3]; RXLANE[0..3])** | | | | | | |
| Differential Input Amplitude (pk – pk ) | $V_{IN_XAUI}$ | 200 | | 2500 | mV | AC Coupled |
| Differential Output Amplitude (pk – pk ) | $V_{OUT_XAUI}$ | 800 | | 1600 | mV | AC Coupled |
| **C.** | | | | | | |
| **MDIO I/O DC Charateristics (MDIO; MDC)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.2 | V | $I_{OL}$=100uA |
| Output Low Current | $I_{OL}$ | | | 4 | mA | |
| Input High Voltage | $V_{IH}$ | 0.84 | | 1.2 | V | |
| Input Low Voltage | $V_{IL}$ | | | 0.36 | V | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Pull-Up Supply Voltage | $V_{PU}$ | 1.152 | 1.2 | 1.248 | V | |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Load Capacitance | $C_{LOAD}$ | | | 470 | pF | |
| External Pull-Up Resistance | $R_{PU}$ | 200 | | | Ω | |

**Electrical Characteristics - AC**

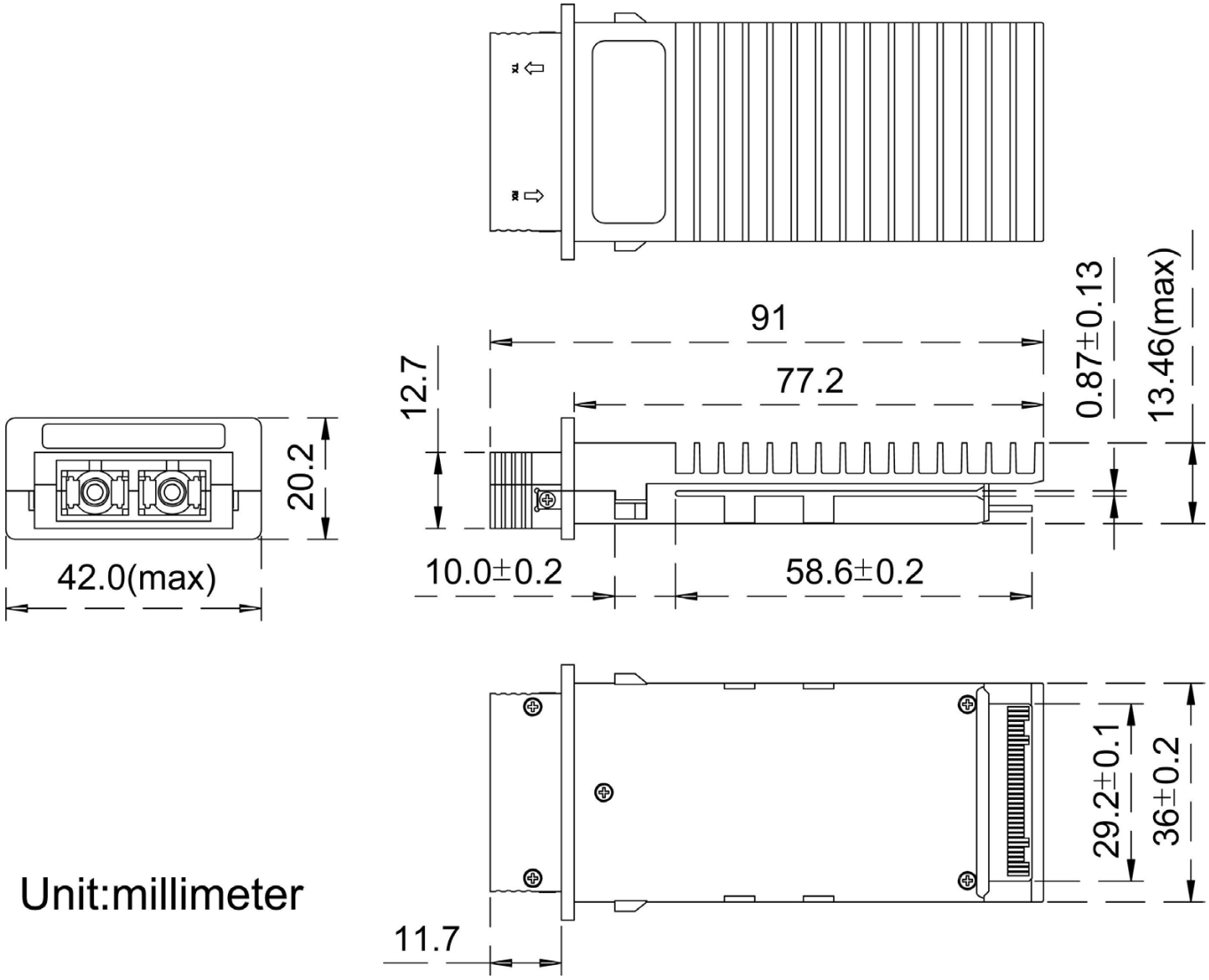
***$V_{CC5}$=4.75V to 5.25V, $V_{CC3}$=3.14V to 3.47V, $V_{CCAPS}$=1.152V to 1.248V, $T_C$=0℃ to 70℃***

| ***Parameter*** | ***Symbol*** | ***Min*** | ***Typ*** | ***Max*** | ***Unit*** | ***Remarks*** |
|---|---|---|---|---|---|---|
| **A.** | | | | | | |
| **XAUI Input AC Characteristics (TXLANE[0..3])** | | | | | | |
| Baud Rate | $BR_{XAUI_IN}$ | | 3.125 | | GBd | |
| Baud Rate Tolerance | $BR_{TOL_XAUI}$ | – 100 | | 100 | ppm | |
| Differential Input Impedance | $Z_{IN_XAUI}$ | 80 | 100 | 120 | Ω | |
| Differential Return Loss | $RL_{IN}$ | 10 | | 1 | dB | 100 MHz to 2.5 GHz |
| Input Differential Skew | $T_{IN_SKEW}$ | | | 75 | ps | Crossing Point |
| Jitter Amplitude Tolerance | $J_{XAUI_TOL}$ | | | 0.65 | $UI_{PP}$ | IEEE 802.3ae |
| **B.** | | | | | | |
| **XAUI Output AC Characteristics (RXLANE[0..3])** | | | | | | |
| Baud Rate | $BR_{XAUI_OUT}$ | | 3.125 | | GBd | |
| Baud Rate Variation | $BR_{XAUI_VAR}$ | – 100 | | 100 | ppm | |
| XAUI Eye Mask (far-end) | According to IEEE 802.3ae | | | | | |
| Output Differential Skew | $T_{OUT_SKEW}$ | | | 15 | ps | |
| Output Differential Impedance | $Z_{OUT_XAUI}$ | 80 | 100 | 120 | Ω | |
| Differential Output Return Loss | $RL_{OUT}$ | 10 | | | dB | 100 MHz to 2.5 GHz |
| Total Jitter | $TJ_{XAUI}$ | | | 0.35 | UI | Near-end No pre-equalization |
| Deterministic Jitter | $DJ_{XAUI}$ | | | 0.17 | UI | 1 UI=320 ps |
| **C.** | | | | | | |
| **Power-On Reset Characteristics** | | | | | | |
| Power-On Reset and TX_ONOFF Characteristics | According to X2 MSA Issue | | | | | |
| **D.** | | | | | | |
| **MDIO I/O AC Characteristics (MDIO; MDC)** | | | | | | |
| MDIO Data Hold Time | $T_{HOLD}$ | 10 | | | ns | |
| MDIO Data Setup Time | $T_{SU}$ | 10 | | | ns | |
| Delay from MDC Rising Edge to MDIO Data Change | $T_{DELAY}$ | | | 300 | ns | |
| MDC Clock Rate | $f_{MAX}$ | | | 2.5 | MHz | |

**Digital Diagnostic**

| ***Parameter*** | ***Symbol*** | ***Min*** | ***Typ*** | ***Max*** | ***Unit*** | ***Remarks*** |
|---|---|---|---|---|---|---|
| Temperature Monitor | $T_{MON}$ | -5 | | +5 | ℃ | |
| Laser Bias Monitor | $I_{MON}$ | -10 | | 10 | % | |
| TX Power Monitor | $P_{TX}$ | -3 | | +3 | dBm | |
| RX Power Monitor | $P_{RX}$ | -3 | | +3 | dBm | |

**Dimensions**




**ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED**

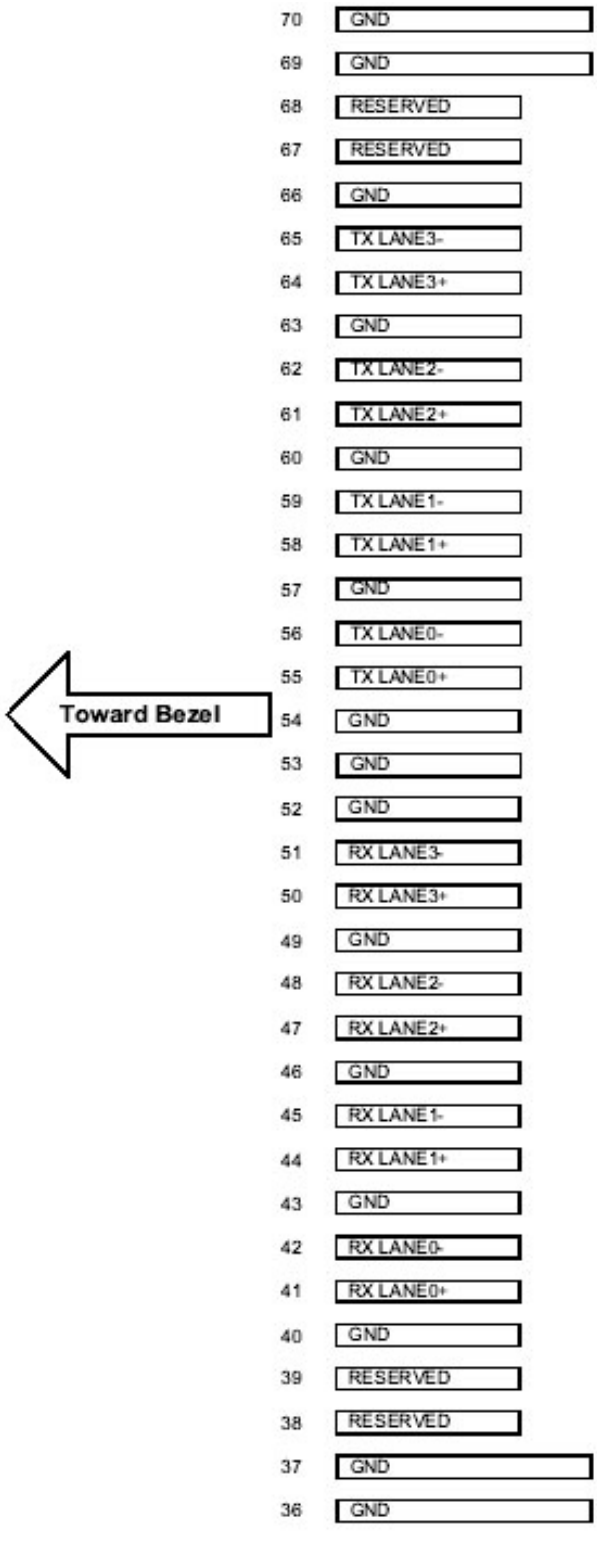
**Pin Assignment – Pin 1 to Pin 35**

| *PIN #* | *Symbol* | *I/O* | *Logic* | *Description* | *Remarks* |
|---|---|---|---|---|---|
| 1 | GND | | Supply | Electrical ground | |
| 2 | GND | | Supply | Electrical ground | |
| 3 | GND | | Supply | Electrical ground | |
| 4 | 5.0V | | Supply | Power | |
| 5 | 3.3V | | Supply | Power | |
| 6 | 3.3V | | Supply | Power | |
| 7 | APS | | Supply | Adaptive Power Supply | |
| 8 | APS | | Supply | Adaptive Power Supply | |
| 9 | LASI | | Open Drain | Link Alarm Status Interrupt. 10-22k ohm pull up on host | |
| 10 | RESET | I | 1.2V CMOS | TX OFF when MDIO RESET | |
| 11 | VEND SPECIFIC | | | Vendor Specific Pin. Leave unconnected | |
| 12 | TX ON/OFF | I | 1.2V CMOS | Transmitter ON/OFF | |
| 13 | RESERVED | | | Reserved | |
| 14 | MOD DETECT | O | | Pulled low inside module through 1k ohm | |
| 15 | VEND SPECIFIC | | | Vendor Specific Pin. Leave unconnected | |
| 16 | VEND SPECIFIC | | | Vendor Specific Pin. Leave unconnected | |
| 17 | MDIO | I/O | Open Drain | Management Data IO | |
| 18 | MDC | I | 1.2V CMOS | Management Data Clock | |
| 19 | PRTAD4 | I | 1.2V CMOS | Port Address bit 4 (Low=0) | |
| 20 | PRTAD3 | I | 1.2V CMOS | Port Address bit 3 (Low=0) | |
| 21 | PRTAD2 | I | 1.2V CMOS | Port Address bit 2 (Low=0) | |
| 22 | PRTAD1 | I | 1.2V CMOS | Port Address bit 1 (Low=0) | |
| 23 | PRTAD0 | I | 1.2V CMOS | Port Address bit 0 (Low=0) | |
| 24 | VEND SPECIFIC | | | Vendor Specific Pin. Leave unconnected | |
| 25 | APS SET | | | Feedback output for APS | |
| 26 | RESERVED | | | Reserved for Avalanche Photodiode use | |
| 27 | APS SENSE | | Analog | APS Sense Connection | |
| 28 | APS | | Supply | Adaptive Power Supply | |
| 29 | APS | | Supply | Adaptive Power Supply | |
| 30 | 3.3V | | Supply | Power | |
| 31 | 3.3V | | Supply | Power | |
| 32 | 5.0V | | Supply | Power | |
| 33 | GND | | Supply | Electrical Ground | |
| 34 | GND | | Supply | Electrical Ground | |
| 35 | GND | | Supply | Electrical Ground | |

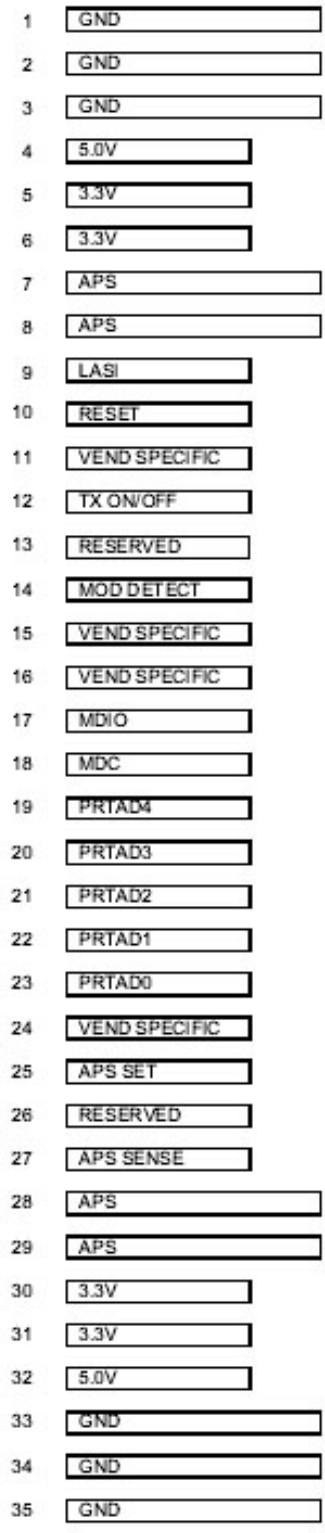
**Pin Assignment – Pin 36 to Pin 70**

| *PIN #* | *Symbol* | *I/O* | *Logic* | *Description* | *Remarks* |
|---|---|---|---|---|---|
| 36 | GND | | Supply | Electrical ground | |
| 37 | GND | | Supply | Electrical ground | |
| 38 | RESERVED | | | Reserved | |
| 39 | RESERVED | | | Reserved | |
| 40 | GND | | Supply | Electrical ground | |
| 41 | RX LANE 0+ | O | AC | Module XAUI Output Lane 0+ | |
| 42 | RX LANE 0– | O | AC | Module XAUI Output Lane 0– | |
| 43 | GND | | Supply | Electrical ground | |
| 44 | RX LANE 1+ | O | AC | Module XAUI Output Lane 1+ | |
| 45 | RX LANE 1– | O | AC | Module XAUI Output Lane 1– | |
| 46 | GND | | Supply | Electrical ground | |
| 47 | RX LANE 2+ | O | AC | Module XAUI Output Lane 2+ | |
| 48 | RX LANE 2– | O | AC | Module XAUI Output Lane 2– | |
| 49 | GND | | Supply | Electrical ground | |
| 50 | RX LANE 3+ | O | AC | Module XAUI Output Lane 3+ | |
| 51 | RX LANE 3– | O | AC | Module XAUI Output Lane 3– | |
| 52 | GND | | Supply | Electrical ground | |
| 53 | GND | | Supply | Electrical ground | |
| 54 | GND | | Supply | Electrical ground | |
| 55 | TX LANE 0+ | I | AC | Module XAUI Input Lane 0+ | |
| 56 | TX LANE 0– | I | AC | Module XAUI Input Lane 0– | |
| 57 | GND | | Supply | Electrical ground | |
| 58 | TX LANE 1+ | I | AC | Module XAUI Input Lane 1+ | |
| 59 | TX LANE 1– | I | AC | Module XAUI Input Lane 1– | |
| 60 | GND | | Supply | Electrical ground | |
| 61 | TX LANE 2+ | I | AC | Module XAUI Input Lane 2+ | |
| 62 | TX LANE 2– | I | AC | Module XAUI Input Lane 2– | |
| 63 | GND | | Supply | Electrical ground | |
| 64 | TX LANE 3+ | I | AC | Module XAUI Input Lane 3+ | |
| 65 | TX LANE 3– | I | AC | Module XAUI Input Lane 3– | |
| 66 | GND | | Supply | Electrical ground | |
| 67 | RESERVED | | | Reserved | |
| 68 | RESERVED | | | Reserved | |
| 69 | GND | | Supply | Electrical Ground | |
| 70 | GND | | Supply | Electrical Ground | |

**Electrical Pad Layout**




**Top of Transceiver PCB**




**Bottom of Transceiver PCB**
**As viewed through top**

**References**

1. IEEE standard 802.3. IEEE Standard Department, 2002., 10GBASE-ER

2. X2 Multi-Source Agreement (MSA).