Preiminary DATA SHEET

CFORTH-DWDM-XENPAK-xx.xx

DWDM XENPAK Transceiver, 32 wavelengths, SC Connectors, 80km over Single Mode Fiber

C F O R T H - D W D M - X E N P A K - x x . x x Overview

CFORTH-DWDM-XENPAK-xx.xx DWDM 10GBd XENPAK optical transceivers are designed for Storage, IP network and LAN, it is a hot pluggable module in the Z-direction that is mainly usable in typical router/switches line card applications.

The CFORTH-DWDM-XENPAK-xx.xx is a fully integrated 10.3 Gb/s optical transceiver module that consists of ITU 100GHz grid wavelength optical transmitter and APD receiver, XAUI interface, Mux and Demux with clock and data recovery (CDR).
In addition, they comply with the XENPAK Multi Sourcing Agreement (MSA).

Product Features

- Up to 10 GBd bi-directional data links.
- Compliant with IEEE 802.3ae application.
- Compliant with XENPAK MSA.
- Temperature stabilized EML transmitter.
- 100GHz ITU Grid, C Band
- APD Photo-detector.
- XAUI electrical interface: 4 lanes @ 3.125 GBd.
- MDIO, DOM (Digital Optics Monitoring) support.
- Hot Z-Pluggable.
- SC Connectors
- Up to 80km on SMF
- Power Supply: 5V/3.3V/Adaptable Power Supply (APS: 1.2V)
- RoHS Compliance
- Class 1 laser product complies with EN 60825-1
- Operating temperature range: 0℃ to 70℃.

Applications

- DWDM 10 GBd Ethernet

Ordering Information

Part Number	*Description*
CFORTH-DWDM-XENPAK-xx.xx	DWDM XENPAK Transceiver, SC Connectors, SingleMode Fiber 80km (ITU 100GHz Grid)

Product Selection

Product number	Description	ITU channel
CFORTH-DWDM-XENPAK-30.33	10GBASE-DWDM 1530.33 nm XENPAK (100-GHz ITU grid)	59
CFORTH-DWDM-XENPAK-31.12	10GBASE-DWDM 1531.12 nm XENPAK (100-GHz ITU grid)	58
CFORTH DWDM XENPAK 31.90	10GBASE DWDM 1531.90 nm XENPAK (100 GHz ITU grid)	57
CFORTH-DWDM-XENPAK-32.68	10GBASE-DWDM 1532.68 nm XENPAK (100-GHz ITU grid)	56
CFORTH-DWDM-XENPAK-33.47	10GBASE-DWDM 1533.47 nm XENPAK (100-GHz ITU grid)	55
CFORTH-DWDM-XENPAK-34.25	10GBASE-DWDM 1534.25 nm XENPAK (100-GHz ITU grid)	54
CFORTH-DWDM-XENPAK-35.04	10GBASE-DWDM 1535.04 nm XENPAK (100-GHz ITU grid)	53
CFORTH-DWDM-XENPAK-35.82	10GBASE-DWDM 1535.82 nm XENPAK (100-GHz ITU grid)	52
CFORTH-DWDM-XENPAK-36.61	10GBASE-DWDM 1536.61 nm XENPAK (100-GHz ITU grid)	51
CFORTH-DWDM-XENPAK-37.40	10GBASE-DWDM 1537.40 nm XENPAK (100-GHz ITU grid)	50
CFORTH-DWDM-XENPAK-38.19	10GBASE-DWDM 1538.19 nm XENPAK (100-GHz ITU grid)	49
CFORTH-DWDM-XENPAK-38.98	10GBASE-DWDM 1538.98 nm XENPAK (100-GHz ITU grid)	48
CFORTH-DWDM-XENPAK-39.77	10GBASE-DWDM 1539.77 nm XENPAK (100-GHz ITU grid)	47
CFORTH-DWDM-XENPAK-40.56	10GBASE-DWDM 1540.56 nm XENPAK (100-GHz ITU grid)	46
CFORTH-DWDM-XENPAK-41.35	10GBASE-DWDM 1541.35 nm XENPAK (100-GHz ITU grid)	45
CFORTH DWDM XENPAK 42.14	10GBASE DWDM 1542.14 nm XENPAK (100 GHz ITU grid)	44
CFORTH-DWDM-XENPAK-42.94	10GBASE-DWDM 1542.94 nm XENPAK (100-GHz ITU grid)	43
CFORTH-DWDM-XENPAK-43.73	10GBASE-DWDM 1543.73 nm XENPAK (100-GHz ITU grid)	42
CFORTH-DWDM-XENPAK-44.53	10GBASE-DWDM 1544.53 nm XENPAK (100-GHz ITU grid)	41
CFORTH-DWDM-XENPAK-45.32	10GBASE-DWDM 1545.32 nm XENPAK (100-GHz ITU grid)	40
CFORTH-DWDM-XENPAK-46.12	10GBASE-DWDM 1546.12 nm XENPAK (100-GHz ITU grid)	39
CFORTH-DWDM-XENPAK-46 92	10GBASE-DWDM 1546 92 nm XENPAK (100-GHz ITU grid)	38
CFORTH-DWDM-XENPAK-47.72	10GBASE-DWDM 1547.72 nm XENPAK (100-GHz ITU grid)	37
CFORTH-DWDM-XENPAK-48.51	10GBASE-DWDM 1548.51 nm XENPAK (100-GHz ITU grid)	36
CFORTH-DWDM-XENPAK-49.32	10GBASE-DWDM 1549.32 nm XENPAK (100-GHz ITU grid)	35
CFORTH-DWDM-XENPAK-50.12	10GBASE-DWDM 1550.12 nm XENPAK (100-GHz ITU grid)	34
CFORTH-DWDM-XENPAK-50.92	10GBASE-DWDM 1550.92 nm XENPAK (100-GHz ITU grid)	33
CFORTH-DWDM-XENPAK-51.72	10GBASE-DWDM 1551.72 nm XENPAK (100-GHz ITU grid)	32
CFORTH DWDM XENPAK 52.52	10GBASE DWDM 1552.52 nm XENPAK (100 GHz ITU grid)	31
CFORTH-DWDM-XENPAK-53.33	10GBASE-DWDM 1553.33 nm XENPAK (100-GHz ITU grid)	30
CFORTH-DWDM-XENPAK-54.13	10GBASE-DWDM 1554.13 nm XENPAK (100-GHz ITU grid)	29
CFORTH-DWDM-XENPAK-54.94	10GBASE-DWDM 1554.94 nm XENPAK (100-GHz ITU grid)	28
CFORTH-DWDM-XENPAK-55.75	10GBASE-DWDM 1555.75 nm XENPAK (100-GHz ITU grid)	27
CFORTH-DWDM-XENPAK-56.55	10GBASE-DWDM 1556.55 nm XENPAK (100-GHz ITU grid)	26
CFORTH-DWDM-XENPAK-57.36	10GBASE-DWDM 1557.36 nm XENPAK (100-GHz ITU grid)	25
CFORTH-DWDM-XENPAK-58.17	10GBASE-DWDM 1558.17 nm XENPAK (100-GHz ITU grid)	24
CFORTH-DWDM-XENPAK-58.98	10GBASE-DWDM 1558.98 nm XENPAK (100-GHz ITU grid)	23
CFORTH-DWDM-XENPAK-59.79	10GBASE-DWDM 1559.79 nm XENPAK (100-GHz ITU grid)	22
CFORTH-DWDM-XENPAK-60.61	10GBASE-DWDM 1560.61 nm XENPAK (100-GHz ITU grid)	21

Absolute Maximum Ratings

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Storage Ambient Temperature	T_S	– 40		85	℃	
Supply Voltage (5V)	V_5	0		6	V	
Supply Voltage (3.3V)	V_3	0		4	V	
Supply Voltage (APS)	V_{APS}	0		1.5	V	
Optical Receiver Input	P_{IMAX}	-5			dBm	Average

General Specifications

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Data Rate	*DR*		10.3125		GBd	
Bit Error Rate	*BER*			10^{-12}		
Total Power Consumption	*P*			4	W	
Supply Voltage (5V)	V_{CC5}	4.75	5	5.25	V	Operating Environment
Supply Voltage (+3.3V)	V_{CC3}	3.14	3.3	3.47	V	Operating Environment
Supply Voltage (APS)	V_{CCAPS}	1.152	1.2	1.248	V	Operating Environment
Supply Current (5V)	I_{CC5}			350	mA	
Supply Current (+3.3V)	I_{CC3}			300	mA	
Supply Current (APS)	I_{CCAPS}			1000	mA	
Case Operating Temperature	T_C	0		70	℃	

Link Distances

Parameter	*Fiber Type*	*Distance Range (Km)*
10.3125 GBd	9/125um SMF	80

Optical Characteristics - Transmitter

V_{CC5}=4.75V to 5.25V, V_{CC3}=3.14V to 3.47V, V_{CCAPS}=1.152V to 1.248V, T_C=0℃ to 70℃

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Optical Center Wavelength	λ	X-100	X	X+100	pm	Note 1
Launch Power	P_{OUT}	– 1		4	dBm	Average
Launch Power of OFF Transmitter	P_{OUT_OFF}			– 30	dBm	Average
Side Mode Suppression Ratio	*SMSR*	30			dB	
Spectral Width (– 20 dB)	$\Delta\lambda$			0.2	nm	
Optical Extinction Ratio	*ER*	9			dB	
Optical Return Loss Tolerance	ORL_T			12	dB	
Relative Intensity Noise	*RIN*			– 128	dB/Hz	
Transmitter Dispersion Penalty	*TDP*			2	dB	
Eye Mask Definition	According to IEEE 802.3ae					

Note:

1、X = specified ITU Grid wavelength

Optical Characteristics - Receiver

V_{CC5}=4.75V to 5.25V, V_{CC3}=3.14V to 3.47V, V_{CCAPS}=1.152V to 1.248V, T_C=0℃ to 70℃

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Center Wavelength Range	λ_C	1260		1600	nm	
Receive Reflectance	TR_{RX}			– 27	dB	
Loss of Signal Assert Level	P_{LOS_A}	– 30			dBm	
Loss of Signal DeAssert Level	P_{LOS_D}			– 24	dBm	
Loss of Signal Hysteresis	P_{LOS_H}	1			dBm	
Receiver electrical 3dB upper cutoff frequency	FR			12.3	GHz	
Dispersion Tolerance	D	– 500		1600	ps/nm	
Optical Input Power (note)	P_{IN}	– 24		– 7	dBm	OSNR >30dB @ 0.1RBW
Power Penalty	P_p			3	dB	OSNR >30dB @ 0.1RBW

Note: Measured with worst ER; BER<10-12; PRBS31.

OSNR Performance-Receiver

V_{CC5}=4.75V to 5.25V, V_{CC3}=3.14V to 3.47V, V_{CCAPS}=1.152V to 1.248V, T_C=0℃ to 70℃

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Optical Input Power (note)	P_{IN}	– 17		– 7	dBm	OSNR =23dB @ 0.1RBW
OSNR Penalty	O_p			3	dB	OSNR =23dB @ 0.1RBW

Note: Measured with worst ER; BER<10-12; PRBS31.

Electrical Characteristics - DC

V_{CC5}=4.75V to 5.25V, V_{CC3}=3.14V to 3.47V, V_{CCAPS}=1.152V to 1.248V, T_C=0℃ to 70℃

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
A.						
1.2V COMS I/O DC Characteristics (PRTAD; LASI; RESET; TX_ON/OFF)						
External Pull-Up Resistor For Open Drain	R_{PU}	10		22	kΩ	
Output High Voltage	V_{OH}	1			V	
Output Low Voltage	V_{OL}			0.15	V	
Input High Voltage	V_{IH}	0.84		1.2	V	
Input Low Voltage	V_{IL}			0.36	V	
Input Pull-Down Current	I_{PD}	20		120	uA	V_{IN}=1.2V
B.						
XAUI I/O DC Charateristics (TXLANE[0..3]; RXLANE[0..3])						
Differential Input Amplitude (pk – pk)	V_{IN_XAUI}	200		2500	mV	AC Coupled
Differential Output Amplitude (pk – pk)	V_{OUT_XAUI}	800		1600	mV	AC Coupled
C.						
MDIO I/O DC Charateristics (MDIO; MDC)						
Output Low Voltage	V_{OL}			0.2	V	I_{OL}=100uA
Output Low Current	I_{OL}			4	mA	

Input High Voltage	V_{IH}	0.84		1.2	V	
Input Low Voltage	V_{IL}			0.36	V	
Pull-Up Supply Voltage	V_{PU}	1.152	1.2	1.248	V	
Input Capacitance	C_{IN}			10	pF	
Load Capacitance	C_{LOAD}			470	pF	
External Pull-Up Resistance	R_{PU}	200			Ω	

Electrical Characteristics - AC

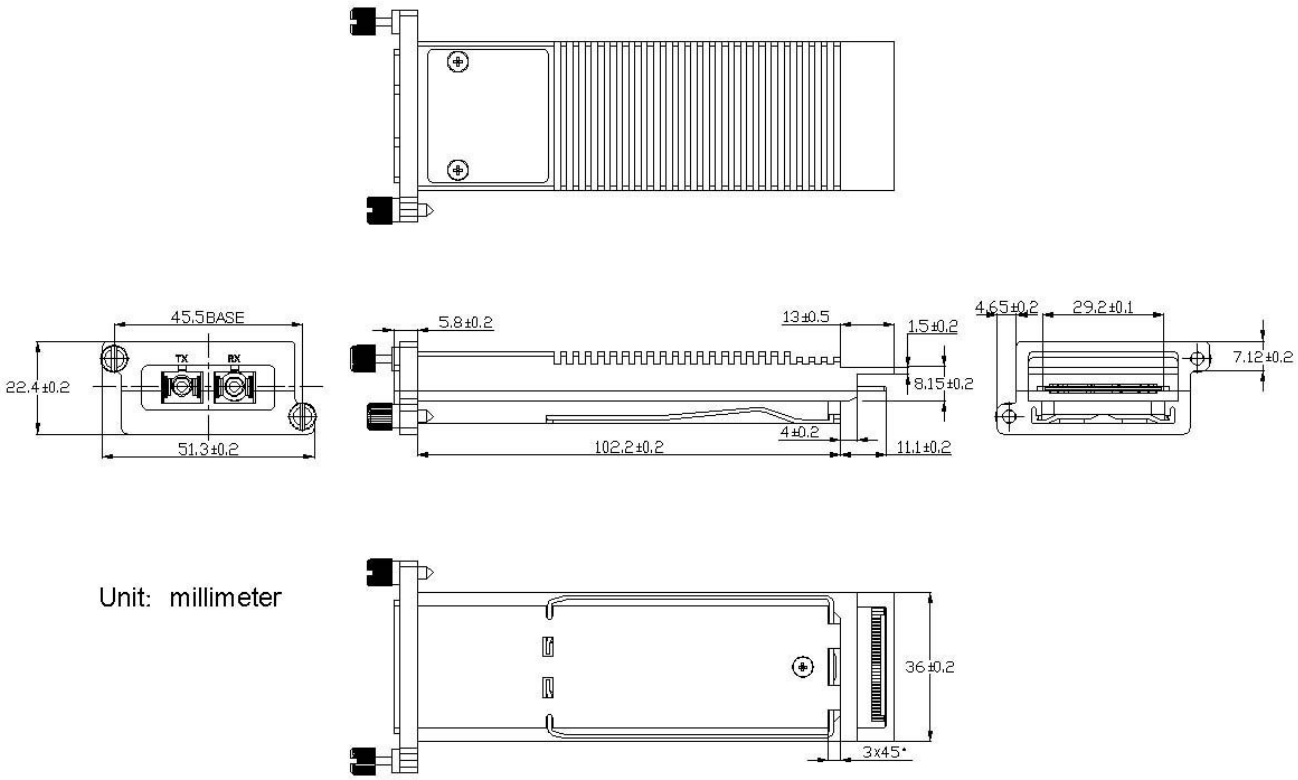
V_{CC5}=4.75V to 5.25V, V_{CC3}=3.14V to 3.47V, V_{CCAPS}=1.152V to 1.248V, T_C=0℃ to 70℃

Parameter	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Remarks***
A.						
XAUI Input AC Characteristics (TXLANE[0..3])						
Baud Rate	BR_{XAUI_IN}		3.125		GBd	
Baud Rate Tolerance	BR_{TOL_XAUI}	– 100		100	ppm	
Differential Input Impedance	Z_{IN_XAUI}	80	100	120	Ω	
Differential Return Loss	RL_{IN}	10			dB	100 MHz to 2.5 GHz
Input Differential Skew	T_{IN_SKEW}			75	ps	Crossing Point
Jitter Amplitude Tolerance	J_{XAUI_TOL}			0.65	UI_{PP}	IEEE 802.3ae
B.						
XAUI Output AC Characteristics (RXLANE[0..3])						
Baud Rate	BR_{XAUI_OUT}		3.125		GBd	
Baud Rate Variation	BR_{XAUI_VAR}	– 100		100	ppm	
XAUI Eye Mask (far-end)	According to IEEE 802.3ae					
Output Differential Skew	T_{OUT_SKEW}			15	ps	
Output Differential Impedance	Z_{OUT_XAUI}	80	100	120	Ω	
Differential Output Return Loss	RL_{OUT}	10			dB	100 MHz to 2.5 GHz
Total Jitter	TJ_{XAUI}			0.35	UI	Near-end No pre-equalization
Deterministic Jitter	DJ_{XAUI}			0.17	UI	1 UI=320 ps
C.						
Power-On Reset Characteristics						
Power-On Reset and TX_ONOFF Characteristics	According to XENPAK MSA Issue					
D.						
MDIO I/O AC Characteristics (MDIO; MDC)						
MDIO Data Hold Time	T_{HOLD}	10			ns	
MDIO Data Setup Time	T_{SU}	10			ns	
Delay from MDC Rising Edge to MDIO Data Change	T_{DELAY}			300	ns	
MDC Clock Rate	f_{MAX}			2.5	MHz	

Digital Diagnostic

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Remarks*
Temperature Monitor	T_{MON}	-5		+5	℃	
Laser Bias Monitor	I_{MON}	-10		10	%	
TX Power Monitor	P_{TX}	-3		+3	dBm	
RX Power Monitor	P_{RX}	-3		+3	dBm	

Dimensions



ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED

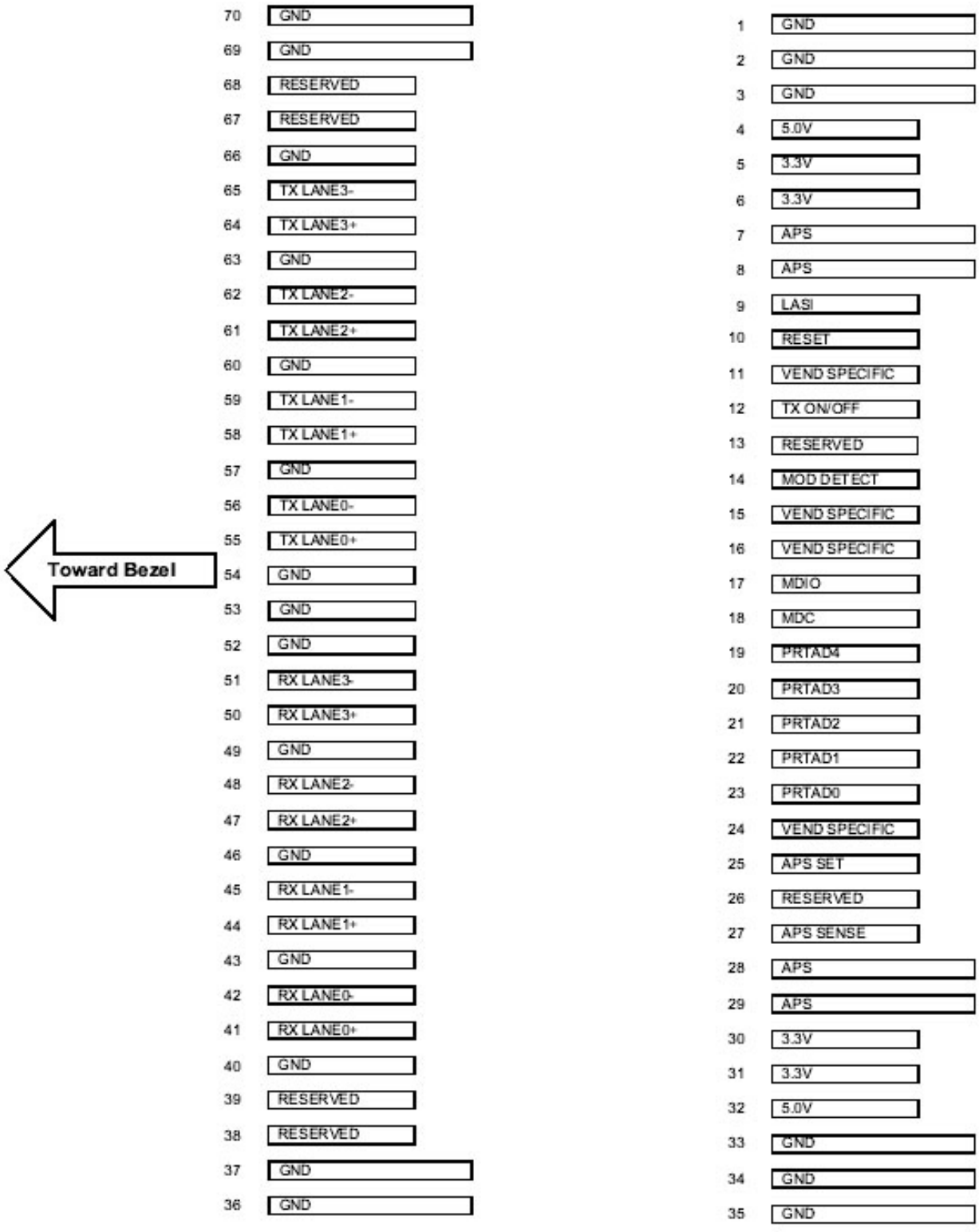
Pin Assignment – Pin 1 to Pin 35

PIN #	*Symbol*	*I/O*	*Logic*	*Description*	*PIN #*
1	GND	I	Supply	Electrical ground	1
2	GND	I	Supply	Electrical ground	2
3	GND	I	Supply	Electrical ground	3
4	5.0V	I	Supply	Power	4
5	3.3V	I	Supply	Power	5
6	3.3V	I	Supply	Power	6
7	APS	I	Supply	Adaptive Power Supply	7
8	APS	I	Supply	Adaptive Power Supply	8
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host	9
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	10
11	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected	11
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	12
13	RESERVED			Reserved	13
14	MOD DETECT	O		Pulled low inside module through 1k ohm	14
15	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected	15
16	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected	16
17	MDIO	I/O	Open Drain	Management Data IO	17
18	MDC	I	1.2V CMOS	Management Data Clock	18
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)	19
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	20
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	21
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	22
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	23
24	VEND SPECIFIC			Vendor Specific Pin. Leave unconnected	24
25	APS SET	O		Feedback output for APS	25
26	RESERVED			Reserved for Avalanche Photodiode use	26
27	APS SENSE	O	Analog	APS Sense Connection	27
28	APS	I	Supply	Adaptive Power Supply	28
29	APS	I	Supply	Adaptive Power Supply	29
30	3.3V	I	Supply	Power	30
31	3.3V	I	Supply	Power	31
32	5.0V		Supply	Power	32
33	GND	I	Supply	Electrical Ground	33
34	GND	I	Supply	Electrical Ground	34
35	GND	I	Supply	Electrical Ground	35

Pin Assignment – Pin 36 to Pin 70

PIN #	*Symbol*	*I/O*	*Logic*	*Description*	*Remarks*
36	GND	I	Supply	Electrical ground	
37	GND	I	Supply	Electrical ground	
38	RESERVED			Reserved	
39	RESERVED			Reserved	
40	GND	I	Supply	Electrical ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0–	O	AC	Module XAUI Output Lane 0–	
43	GND	I	Supply	Electrical ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1–	O	AC	Module XAUI Output Lane 1–	
46	GND	I	Supply	Electrical ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+	
48	RX LANE 2–	O	AC	Module XAUI Output Lane 2–	
49	GND	I	Supply	Electrical ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3–	O	AC	Module XAUI Output Lane 3–	
52	GND	I	Supply	Electrical ground	
53	GND	I	Supply	Electrical ground	
54	GND	I	Supply	Electrical ground	
55	TX LANE 0+	O	AC	Module XAUI Input Lane 0+	
56	TX LANE 0–	O	AC	Module XAUI Input Lane 0–	
57	GND	I	Supply	Electrical ground	
58	TX LANE 1+	O	AC	Module XAUI Input Lane 1+	
59	TX LANE 1–	O	AC	Module XAUI Input Lane 1–	
60	GND	I	Supply	Electrical ground	
61	TX LANE 2+	O	AC	Module XAUI Input Lane 2+	
62	TX LANE 2–	O	AC	Module XAUI Input Lane 2–	
63	GND	I	Supply	Electrical ground	
64	TX LANE 3+	O	AC	Module XAUI Input Lane 3+	
65	TX LANE 3–	O	AC	Module XAUI Input Lane 3–	
66	GND	I	Supply	Electrical ground	
67	RESERVED			Reserved	
68	RESERVED			Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	

Electrical Pad Layout



Top of Transceiver PCB

Bottom of Transceiver PCB
As viewed through top

References

1. IEEE standard 802.3. IEEE Standard Department, 2005.

2. XENPAK Multi-Source Agreement (MSA).